We claim:

1. A microprocessor system comprising a CPU, a clock providing a CLK signal to the CPU, a counter counting clock pulses to the CPU, and a monitor, wherein the clock is adapted to provide a CLK signal to the counter when a software task is running on the CPU, said counter adapted to count the number of clock pulses since a RESET; the CPU is adapted to provide a RESET signal to the counter for each CLK pulse when a software task is not running on the CPU; and the monitor is adapted to store the value in the counter immediately prior to the last RESET.

2. The microprocessor system of claim 1 wherein the CPU is adapted to block a RESET signal to the counter when a software task is running on the CPU.

3. The microprocessor system of claim 1 wherein the CPU is adapted to continuously pass CLK signals to the counter when a software task is running on the CPU.

4. The microprocessor system of claim 1 wherein the CPU is adapted to pass a RESET signal to the counter when is software task is not running on the CPU.

5. The microprocessor system of claim 1 wherein the monitor is adapted to output a control signal responsive to monitor content.

6. The microprocessor system of claim 5 wherein the monitor is adapted to output a power control signal responsive to monitor content.

7. The microprocessor system of claim 5 wherein the monitor is adapted to output a function control signal responsive to monitor content.

8. The microprocessor system of claim 5 wherein the monitor is adapted to output a clock control signal responsive to monitor content.

9. The microprocessor system of claim 5 wherein the monitor is adapted to output a control signal reducing power input to the CPU responsive to monitor content when the monitor content is below a threshold.

10. The microprocessor system of claim 5 wherein the monitor is adapted to output a control signal reducing clock pulse input to the CPU responsive to count content when the monitor content is below a threshold.

11. A method of operating a microprocessor system, said system comprising a CPU, a counter, a monitor, and a clock, and wherein the clock provides a CLK signal train to the counter while a software task is running on the CPU, the counter counting the number of clock pulses since a RESET, the CPU providing a RESET signal to the counter for each CLK pulse when a software task is not running on the CPU, and the monitor storing the value of the counter prior to the last RESET.

12. The method of claim 11 wherein the CPU blocks the RESET signal to the counter when a software task is running on the CPU.

13. The method of claim 11 wherein the CPU continuously passes CLK signals to the counter when a software task is running on the CPU.

14. The method of claim 11 wherein the CPU passes a RESET signal to the counter when is software task is not running on the CPU.

15. The method of claim 11 wherein the monitor outputs a control signal responsive to count content.

16. The method of claim 15 wherein the monitor outputs a power control signal responsive to monitor content.

17. The method of claim 15 wherein the monitor outputs a function control signal responsive to monitor content.

18. The method of claim 15 wherein the monitor outputs a clock control signal responsive to monitor content.

19. The method of claim 15 wherein the monitor outputs a control signal reducing power input to the CPU responsive to monitor content when the monitor content is below a threshold.

20. The method of claim 15 wherein the monitor outputs a control signal reducing clock speed of the CPU responsive to monitor content when the monitor content is below a threshold.